May Tapeout

What’s on the Chip?

* n = 1, 4, 9 (maybe 16) CLBs
  + Base case and Custom Case
  + Comparison points
    - Delay
    - Energy
    - Area (floorplan and # of transistors)
    - # of config bits
* Configure 1 CLB (n=1, base case), connected to 4 wires (1 channel)
  + LUTs
  + Muxes
  + Register
  + Connection Box

Necessary Pins

* ScanIn - for configuration
* VDD
* VDDc - measure config bit power
* VDDIO
* VSS
* +/- terminals to measure delay, resistance, and capacitance for:
  + Metal Wires
  + Switch Box
  + Connection Box
  + Sense Amp
  + Driver
  + Intra-CLB data path - look at VPR manual to see where those need to be

Questions/Thoughts:

* Capacitance Measurement?
  + Delay\*I/V? Delay/(0.69R)?
* Delay/Resistance/Capacitance measurements are for making architecture files to match up with our design

Importance for August:

* Proof of ability to tape out mini-FPGA CLBs
* Hardware characterization of different delay paths associated with the CLBs
* First attempt at configuration of a small chunk of an FPGA (Just the CLB)
* Tapeout experience before the potential full chip
* Sets timeline on configuration/CLB choice early in the process

Importance for FPGA Research in General

* Potential for increased optimization for Low Power FPGAs
  + Goal - optimize each piece of the FPGA individually
* Hardware evidence (along with simulation and analytical evidence) for a more complete design space exploration of mux-based vs. mini-FPGA CLBs
* Development of custom bitstream generation tools (and perhaps a more generalized, scalable version of previous software)
* Extracted Models (Resistance, Capacitance, Timing) that can be used in CAD tools